App. Ser. No. 09/740,174
Atty. Dkt. No. MIO 0042 V2

IN THE SPECIFICATION

Please replace the paragraph beginning on page 20, line 22 with the following rewritten paragraph.

--The first and second pull-up transistors 32 and 36 of the SRAM memory cells 30 making up each row of the memory array 90 are preferably formed within the same N-well as shown in Fig. 7. Four N-wells 64_1-64_4 with each of the first and second pull-up transistors 32 and 36~~34~~ for each memory cell 30 in each row sharing a respective N-well are shown in Fig. 7. For illustrative purposes, the two horizontal boxes of each cell represent the gate connections for each pull-up transistor 32, 36~~34~~ while the vertical box represents the active areas for the transistors 32, 36~~34~~. It will be appreciated by those skilled in the art that the first and second pull-down transistors 34~~36~~, 38 for each memory cell 30 would be appropriately formed on both sides of the respective N-wells 64_1-64_4.--

E'